CLAIMS

What is claimed is:

1. A slew rate control circuit, comprising:

an input voltage node;

an output voltage node coupleable to a load;

a first circuit node;

a first transistor having a gate, a source, and a drain, the drain of the first transistor being coupled to the output voltage node, the source of the first transistor being coupleable to a first voltage source, wherein the first transistor is biased to operate within its active operating region;

a feedback resistor having first and second terminals coupled to the output voltage node and the first circuit node, respectively, the feedback resistor being connected between the gate and the drain of the first transistor; and

an input resistor having first and second terminals coupled to the second terminal of the feedback resistor and the input voltage node, respectively,

wherein the control circuit is operative to provide a ramped down voltage signal at the output voltage node that linearly tracks a first ramped up voltage signal applied to the input voltage node.

2. The control circuit of claim 1 wherein the first transistor is an NMOS transistor.

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3. The control circuit of claim 1 wherein the ramped down voltage signal provided at the output voltage node ramps down from 0 volts to a first negative voltage level.

4. The control circuit of claim 3 wherein the first voltage source is operative to provide a voltage level equal to the first negative voltage level.

5. The control circuit of claim 3 wherein the first ramped up voltage signal applied to the input voltage node ramps up from a second negative voltage level to 0 volts.

6. The control circuit of claim 5 wherein the first negative voltage level equals the second negative voltage level.

7. The control circuit of claim 1 further including level shifting circuitry coupled between the second terminal of the input resistor and the input voltage node.

8. The control circuit of claim 7 wherein the level shifting circuitry is operative to level shift a second ramped up voltage signal applied to the input voltage node to the first ramped up voltage signal provided at the second terminal of the input resistor.

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9. The control circuit of claim 8 wherein the second ramped up voltage signal applied to the input voltage node ramps up from 0 volts to a first positive voltage level.

10. The control circuit of claim 1 further including a bias current source coupled to the gate of the first transistor, the bias current source being operative to bias the first transistor within its active operating region.

11. The control circuit of claim 1 further including a controlled bias current source coupled to the gate of the first transistor, the controlled bias current source being operative to bias the first transistor within its active operating region by applying a controlled current to the gate of the first transistor.

12. The control circuit of claim 11 wherein the controlled bias current source is operative to apply the controlled current to the gate of the first transistor after the first ramped up voltage signal ramps to a predetermined voltage level, thereby reducing an on-resistance between the drain and the source of the first transistor.

13. The control circuit of claim 12 wherein the controlled bias current source is operative to apply the

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controlled current to the first transistor gate in sequenced steps.

14. The control circuit of claim 11 wherein the controlled bias current source is operative to apply the controlled current to the gate of the first transistor after the first ramped up voltage signal ramps to a predetermined voltage level and after a predetermined time delay, thereby reducing an on-resistance between the drain and the source of the first transistor.

15. The control circuit of claim 14 wherein the controlled bias current source is operative to apply the controlled current to the first transistor gate in sequenced steps.

16. The control circuit of claim 11 wherein the controlled bias current source is operative to sequentially increase a level of the controlled current applied to the first transistor gate from a first current level to at least one second current level greater than the first current level after the first ramped up voltage signal ramps to a predetermined voltage level.

17. The control circuit of claim 11 wherein a combination of the first transistor and the feedback resistor forms a closed control loop, and further including a controllable switch disposed within the control loop, the switch being controllable to open

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before the controlled current is applied to the gate of the first transistor by the controlled bias current source.

18. The control circuit of claim 1 further including a third resistor coupled between the first circuit node and the gate of the first transistor, wherein a voltage across the third resistor is operative to provide compensation for a voltage across the gate and the source of the first transistor.

19. A method of controlling a slew rate of an output supply, comprising the steps of:

providing a first transistor having a gate, a source, and a drain, the drain of the first transistor being coupled to an output voltage node, the source of the first transistor being coupleable to a first voltage source;

providing a feedback resistor having first and second terminals coupled to the output voltage node and a first circuit node, respectively, the feedback resistor being connected between the gate and the drain of the first transistor;

providing an input resistor having first and second terminals coupled to the second terminal of the feedback resistor and an input voltage node, respectively;

applying a first ramped up voltage signal to the input voltage node; and

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providing a ramped down voltage signal at the output voltage node that linearly tracks the first ramped up voltage signal.

20. The method of claim 19 further including the step of biasing the first transistor to operate within its active operating region by a bias current source.

21. The method of claim 19 wherein the first transistor is an NMOS transistor.

22. The method of claim 19 wherein the fourth providing step includes providing a ramped down voltage signal that ramps down from 0 volts to a first negative voltage level.

23. The method of claim 22 further including the step of providing a voltage level equal to the first negative voltage level by the first voltage source.

24. The method of claim 22 wherein the applying step includes applying a first ramped up voltage signal ramps up from a second negative voltage level to 0 volts.

25. The method of claim 24 wherein the first negative voltage level equals the second negative voltage level.

26. The method of claim 19 further including the step of providing level shifting circuitry coupled between the

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second terminal of the input resistor and the input voltage node.

27. The method of claim 26 further including the step of level shifting a second ramped up voltage signal applied to the input voltage node to the first ramped up voltage signal provided at the second terminal of the input resistor by the level shifting circuitry.

28. The method of claim 27 wherein the second ramped up voltage signal applied to the input voltage node ramps up from 0 volts to a first positive voltage level.

29. The method of claim 19 further including the step of providing a third resistor coupled between the first circuit node and the gate of the first transistor.

30. The method of claim 29 wherein a voltage across the third resistor provides compensation for a voltage across the gate and the source of the first transistor.

31. The method of claim 19 further including the steps of providing a controlled bias current source coupled to the gate of the first transistor, and applying a controlled current to the gate of the first transistor by the controlled bias current source to bias the first transistor within its active operating region.

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32. The method of claim 31 wherein the second applying step includes applying the controlled current to the gate of the first transistor after the first ramped up voltage signal ramps to a predetermined voltage level, thereby reducing an on-resistance between the drain and the source of the first transistor.

33. The method of claim 32 wherein the second applying step includes applying the controlled current to the first transistor gate in sequenced steps.

34. The method of claim 31 wherein the second applying step includes applying the controlled current to the gate of the first transistor after the first ramped up voltage signal ramps to a predetermined voltage level and after a predetermined time delay, thereby reducing an on-resistance between the drain and the source of the first transistor.

35. The method of claim 34 wherein the second applying step includes applying the controlled current to the first transistor gate in sequenced steps.

36. The method of claim 31 wherein the second applying step includes sequentially increasing a level of the controlled current applied to the first transistor gate from a first current level to at least one second current level greater than the first current level after the

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first ramped up voltage signal ramps to a predetermined voltage level.

37. The method of claim 31 wherein a combination of the first transistor and the feedback resistor forms a closed control loop, and further including providing a controllable switch disposed within the control loop, the switch being controllable to open before the controlled current is applied to the gate of the first transistor by the controlled bias current source.

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